IN THE DRAWINGS

Please replace current **Figures 3, 25, 27, 29, 30A, 34, 37, 39, 40, 43** and **48B** with revised **Figures 3, 25, 27, 29, 30A, 34, 37, 39, 40, 43** and **48B**. Clean copies of the revised figures are enclosed. Redlined versions have not been submitted, since the only requested revision was the modification of top margins. The Applicants respectfully request approval of the proposed amended figures.

IN THE SPECIFICATION

Please amend the written specification for the above-identified patent application as follows:

Please replace the application title with the following title:

METHOD AND APPARATUS FOR QUANTIFYING THE QUALITY OF PLACEMENT CONFIGURATIONS IN A PARTITIONED REGION OF AN INTEGRATED CIRCUIT LAYOUT

IN THE CLAIMS

Please amend the claims in the above-identified patent application as follows:

28. (Amended) A method of placing circuit modules in a region of an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements,

wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) partitioning the IC region into several sub-regions, wherein a plurality of edges exist between said sub-regions, wherein a plurality of said edges are diagonal;

b) selecting a net;

c) identifying the set of sub-regions containing the circuit elements of the selected net;

d) identifying the edges, from the plurality of edges, intersected by at least one connection graph that represents a topology of one or more interconnect lines necessary for connecting the identified set of sub-regions, wherein at least one of the identified edges is diagonal; and

e) computing a placement cost by using the identified edges.

29. (Amended) The method of claim 28, wherein a plurality of said edges are horizontal and a plurality are vertical.

31. (Amended) The method of claim 30, wherein the plurality of edges are defined based on a wiring model for the IC layout and on a partitioning structure defined by the partitioning lines.

43. (Amended) A method of placing circuit modules in a region of an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements, wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) partitioning the IC region into several sub-regions, wherein a plurality of line paths exist between said sub-regions, wherein a plurality of said line paths are diagonal;

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b) selecting a net;

c) identifying the set of sub-regions containing the circuit elements of the selected net;

d) identifying the plurality of line paths used by at least one connection graph that represents a topology of one or more interconnect lines necessary for connecting the identified set of sub-regions, wherein at least one of the identified line paths is diagonal; and

e) computing a placement cost by using the identified line paths.

44. (Amended) The method of claim 43, wherein a plurality of said line paths are horizontal and a plurality are vertical.

58. (Amended) For an electronic-design-automation placer that uses a set of partitioning lines, that define a plurality of slots, to partition an integrated-circuit ("IC") layout region into a plurality of sub-regions corresponding to said slots, wherein a

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plurality of line paths exist between said slots, a method of pre-computing costs of placing circuit modules in an IC layout region, the method comprising:

a) for each combination of said slots, identifying at least one connection graph that represents a topology of interconnect lines necessary for connecting the combination of said slots;

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b) for each combination of said slots, identifying the line paths used by the connection graph or graphs for that particular combination of slots, wherein a plurality of the identified line paths are diagonal; and

c) storing the plurality of identified line paths for each combination of slots in a storage structure.

59. (Amended) The method of claim 58, wherein a plurality of the line paths are horizontal, and a plurality are vertical.

67. (Amended) For an electronic-design-automation placer that uses a set of partitioning lines, that define a plurality of slots, to partition an integrated-circuit ("IC") layout region into a plurality of sub-regions corresponding to said slots, wherein a plurality of edges exist between said slots, a method of pre-computing costs of placing circuit modules in an IC layout region, the method comprising:

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a) for each combination of said slots, identifying at least one connection graph that represents a topology of interconnect lines necessary for connecting the combination of said slots;